sub A2

ABSTRACT

A method is provided for an integrated circuit interconnect having a dielectric layer disposed between a wide top metal line and a wide bottom metal line. A via-sea in the dielectric layer connects the wide top and wide bottom metal lines by means of a first via having a width, a second via having a width and spaced more than a width away and less than four widths away from the first via. The width and spacing of the vias reduce the occurrence of metal explosions which are known to reduce the power carrying capability of the power lines and adversely affect the performance of the devices in the integrated circuit.